IN THE CLAIMS

1. (Currently amended) A capacitor formed on a semiconductor substrate, the capacitor comprising:

a first electrode region of a first stair-stepped metal layer;

a contact region of the first stair-stepped metal layer;

a second electrode of a second metal layer that is closer to the substrate than the first stair-stepped metal layer;

a dielectric layer intermediate the first electrode region and the second electrode, the dielectric layer including a contact opening therethrough in the vicinity of the contact region,

wherein the first stair-stepped metal layer in a stair-stepped region thereof steps laterally and downwardly across the dielectric layer and into and at least partway laterally across the contact opening; and

a wire electrically coupled to and in contact with a bottom surface of the contact region of the first stair-stepped metal layer through the contact opening in the dielectric layer,

wherein the first electrode region is electrically coupled to the wire through the contact opening in the dielectric layer.

2. (Original) The capacitor of claim 1 wherein the wire is formed of a third metal layer that is closer to the substrate than the second metal layer.

3. (Original) The capacitor of claim 1 wherein the wire is formed of the second metal layer.

4. (Cancelled)

5. (Previously presented) The capacitor of claim 1 wherein the contact opening comprises a plurality of separate contact holes.

6. (Original) The capacitor of claim 1 wherein the wire has a planarized top surface.

7. (Original) The capacitor of claim 6 wherein the wire comprises a damascene layer.

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Currently amended) A metal-insulator-metal capacitor, comprising:

a wire layer formed in a first metal layer, the wire layer including a first electrode contacting line;

a bottom electrode formed in a second metal layer;

wherein the wire layer comprises a second electrode contacting line, and wherein the second electrode contacting line is coupled to a bottom surface of the bottom electrode;

a top electrode formed in a third metal layer, the top electrode disposed over the bottom electrode;

a dielectric layer separating the bottom electrode from the top electrode;

a contact formed between the first electrode contacting line and a bottom side of the top electrode; and

a second contact located on a top side of the bottom electrode,

wherein a portion of the bottom surface of the bottom electrode directly contacts a top surface of the second electrode contacting line and not through a contact hole[[.]], and

wherein a portion of the bottom surface of the bottom electrode directly contacts a top surface of the second electrode contacting line and not through a contact hole.

13. (Previously presented) The capacitor of claim 12 wherein the bottom electrode couples to the second electrode contacting line through a contact hole in an insulation layer.

14. (Previously presented) The capacitor of claim 12 wherein the first and second electrode contacting lines each have a planarized top surface.

15. (Original) The capacitor of claim 14 wherein the first and second contacting lines are planarized by a damascene process.

16. (Original) The capacitor of claim 14 wherein the first and second contacting lines are planarized by a CMP process performed on an interlayer dielectric layer.

17. (Previously presented) The capacitor of claim 12 wherein a top surface of the first and second contacting lines are formed in a process other than planarization.

18. (Cancelled)

19. (Currently amended) The capacitor of claim 12[[8]], wherein the second contact extends away from a[[the]] substrate farther than the third metal layer.

20. (Currently amended) A metal-insulator-metal capacitor, comprising:

a first metal layer including a bottom electrode and an electrode contacting line;

a top stair-stepped electrode formed in a second metal layer, the top electrode disposed over the bottom electrode;

a dielectric layer separating the bottom electrode from the top electrode;

a contact formed between the electrode contacting line and a bottom side of the top electrode; and

a second contact located on a top side of the bottom electrode.

21. (Previously presented) A metal-insulator-metal capacitor, comprising:

a first metal layer including a bottom electrode and an electrode contacting line;

a top electrode formed in a second metal layer, the top electrode disposed over the bottom electrode;

a dielectric layer separating the bottom electrode from the top electrode;

a contact formed between the electrode contacting line and a bottom side of the top electrode; and

a second contact located on a top side of the bottom electrode,

wherein the top electrode couples to the electrode contacting line through a contact hole in the dielectric layer.

22. (Original) The capacitor of claim 21, wherein the contact hole comprises a plurality of separate holes.

23. (Cancelled)

24. (Currently amended) The capacitor of claim 21, wherein the second contact extends away from a[[the]] substrate farther than the second metal layer.

25. (Previously presented) The capacitor of claim 21 wherein the bottom electrode and the electrode contacting line each have a planarized top surface.

26. (Original) The capacitor of claim 25 wherein the bottom electrode and the electrode contacting line are planarized by a damascene process.

27. (Original) The capacitor of claim 25 wherein the bottom electrode and the electrode contacting line are planarized by a CMP process performed on an interlayer dielectric layer.

28. (Previously presented) The capacitor of claim 21 wherein the bottom electrode and the electrode contacting line are formed in a process other than planarization.

29-51. (Cancelled)

52. (Currently amended) A metal-insulator-metal capacitor, comprising:

a wire layer formed in a first metal layer, the wire layer including a first electrode contacting line;

a bottom electrode formed in a second metal layer;

a stair-stepped top electrode formed in a third metal layer, the top electrode disposed over the bottom electrode;

a dielectric layer separating the bottom electrode from the top electrode; and

a contact formed between the electrode contacting line and a bottom side of the top electrode, wherein the top electrode couples to the first electrode contacting line through a contact hole in the dielectric layer, the contact hole having a vertical:horizontal aspect ratio of less than about 1:1.